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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/314,750	05/19/1999	HIROSHI MURAKAMI	0941.63081	5601

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EXAMINER	
LESPERANCE, JEAN E	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 12/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/314,750	MURAKAMI, HIROSHI	
	Examiner	Art Unit	
	Jean E Lesperance	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6 and 8-11* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 May 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

ETAILED ACTION

1. The amendment filed October 23, 2006 is entered and claims 2-11 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 2-11 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

3. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Objections

4. Claim 2 is objected to because of the following informalities: information sorted in line 19 is supposed to be "information stored". Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 6, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent # 5,912,651 ("Bitzakidis et al.") in view of Us Patent # 5,333,261 ("Guttag et al.").

As for claim 2, Ikeda et al. teach a display device (Fig.1 (10)) comprising:

a display unit, which displays an image (display panel, Fig.1 (10));

a display-data line, which supplies data of the image from an exterior of said display unit (the lines 1, 2,...n, which are connected between the circuit 22 and the display panel Fig.1 (10));

an operation circuit unit which controls said display unit to display the data of the image supplied through said display data line based on the information stored in said memories (the timing and control circuit (21) connected to the row driver circuit (20) and the data driver (22));

a data bus which connects said memories to an exterior of said display device and supplies the information to said memories from the exterior of said display device (the bus that connects the video processing circuit (24) to the column driver (22) where the column driver circuit is exterior to the display panel (10); and

an address bus which connects said memories to the exterior of said display device, and supplies address signals for selecting one of said memories (the bus that connects the timing and control circuit (21) to the row driver circuit (20) where the row driver circuit is exterior to the display panel (10);

wherein said operation circuit unit (the timing and control circuit (21) connected to the row driver circuit (20) and the data driver (22)) includes:

the data which drives the data lines of said display unit, wherein at least one of said gate driver and said data driver operates based on the information stored on said memories (the column driver circuit (22) comprising one or more shift register/sample and hold circuits, where the memory in the shift register in the row driver circuit);

a gate driver which drives gate lines of said display unit wherein at least one of said gate driver and said data driver operates based on the information stored said memories (the row driver circuit (20) comprising a digital shift register controlled by regular timing pulses from a timing where the shift register is inherently can be used to store information to control the row driver circuit (20)). Accordingly, the prior art teaches all the claimed limitations with the exception of providing memories which store information for controlling displaying of the data of the image on said display unit, said information being different from said data of the image.

However, Guttag et al. teach The X Y addressing mode is most useful for that portion of video RAM 132 which includes the bit map data, called the screen memory which is the portion of memory which controls the display (column 8, line 67 to column 9, line 2), where FIG. 7 illustrates video RAM 132 which includes screen memory 705 and off screen memory 715 (column 11, lines 4-6) where 705 and 715 corresponding to memories.

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the RAM 132 as taught by Guttag et al. in the matrix display disclosed by Bitzakidis et al. because this would provide a mask to extract one of the coordinates from the address data word (column 2, lines 41 and 42).

As for claim 3, Bitzakidis et al. teach at least one of said gate driver and said data driver includes a shift register which operates based on the information stored in said memories to control a scan direction of said display unit (the row driver circuit (20) comprising a digital shift register controlled by regular timing pulses from a timing and control circuit (21) and the column driver circuit (22) comprising one or more shift register/sample and hold circuits, where the memory in the shift register in the row driver circuit and the column driver circuit is different to the memory coming from the data processing circuit (24)).

As for claim 6, Bitzakidis et al. teach memories store pattern data, said data driver operating in accordance with the pattern data stored in said memories to control said display unit to display an image corresponding to the pattern data (the column driver circuit (22) comprising one or more shift register/sample and hold circuits, where the memory in the shift register in the row driver circuit and the column driver circuit is different to the memory coming from the data processing circuit (24)).

As for claim 8, Bitzakidis et al. teach to a display-information acquisition circuit which acquires information about said display unit (panel illuminating means (19), is operated by driving the rows of picture elements such that the display information of successive fields of an applied video signal is written into the panel in respective panel display information address periods that are substantially less than the applied video signal field period and separated by a time interval (abstract)); display-information memories which store the information about said display unit (the row driver circuit (20) comprising a digital shift register controlled by regular timing pulses from a timing and

control circuit (21) and the column driver circuit (22) comprising one or more shift register/sample and hold circuits, where the memory in the shift register in the row driver circuit and the column driver circuit is different to the memory coming from the data processing circuit (24)).

As for claim 9, Bitzakidis et al. teach a display-information acquisition circuit checks said display unit to acquire information about said display unit with regard to a defect of said display unit (panel illuminating means (19), is operated by driving the rows of picture elements such that the display information of successive fields of an applied video signal is written into the panel in respective panel display information address periods that are substantially less than the applied video signal field period and separated by a time interval (abstract)).

As for claim 10, Bitzakidis et al. teach said display data acquisition circuit acquires the information about the said display (panel illuminating means (19), is operated by driving the rows of picture elements such that the display information of successive fields of an applied video signal is written into the panel in respective panel display information address periods that are substantially less than the applied video signal field period and separated by a time interval (abstract)).

As for claim 11, Bitzakidis et al. teach a plurality of pixel electrodes corresponding to the respective polysilicon thin film transistor. It is well know in the art to have a polysilicon thin film transistor.

6. Claims 4 and 5 are rejected under 35 U. S. C. 103 (a) as being unpatentable

over U. S. Patent # 5,912,651 ("Bitzakidis et al.") in view of Us Patent # 5,333,261 ("Guttag et al.") and in further view of US Patent # 5,712652 ('Sato et al.').

As for claim 4, the combination of Bitzakidis et al. and Guttag et al. teaches all the claimed limitation with the exception of providing at least one of said gate driver and said data driver includes a decoder which operates based on the information stored in said memories to control a scan direction and a scan order of said display unit.

However, Sato et al. teach a decoder type liquid crystal drive circuit system, that is, a data driver 501 and a scan driver 502 are both arranged at the peripheral portion of a picture display region in which the pixels are arranged. In these decoder 501 and 502, a logical circuit is provided in such a way that line activation signals can be generated whenever the address signals match the respective data lines or the respective scanning lines (column 19, line 62 to column 20, line 2).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the decoder as taught by Sato et al. in the shift register disclosed by the combination of Bitzakidis et al. and Guttag et al. because this would provide a liquid crystal display device which is simple in structure and thereby in the manufacturing process, high in the display density, and therefore suitable for the portable data processing apparatus such as a notebook type personal computer (column 6, lines 1519).

As for claim 5, Sato et al. teach at least one of said gate driver and said data driver further includes an address counter which operates based on the information stored in said memories to supply an address to said decoder, said decoder decoding

the address to control the scan direction and the scan order of said display unit a decoder type liquid crystal drive circuit system, that is, a data driver 501 and a scan driver 502 are both arranged at the peripheral portion of a picture display region in which the pixels are arranged. In these decoder 501 and 502, a logical circuit is provided in such a way that line activation signals can be generated whenever the address signals match the respective data lines or the respective scanning lines (column 19, line 62 to column 20, line 2) where the logical circuit is interpreted as a address counter. See the motivation of claim 4.

7. Claim 11 is rejected under 35 U. S. C. 103 (a) as being unpatentable over U. S. Patent # 5,912,651 ("Bitzakidis et al.") in view of Us Patent # 5,333,261 ("Guttag et al.") and in further view of US Patent # 5818558 ("Ogishima").

As for claim 11, Bitzakidis et al teach a transistor (11) but fail to teach a plurality of polysilicon thin-film transistors and a plurality of pixel electrodes corresponding to the respective polysilicon thin-film transistors, wherein display data is supplied to the pixel electrodes via the polysilicon thin-film transistors selected by said gate driver and said data driver.

However, Ogishma teaches an active-matrix driving LCD provided with an MIM (metal-insulator-metal) or a thin-film transistor made of amorphous silicon, polysilicon, single crystalline silicon (column 9, lines 45-48) where in Fig.3, the transistor TT is connected to the gate driver line and data driver line to provide the display data to the pixel electrode 2B.

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize the transistor as taught by Ogishima in the display panel disclosed by Bitzakidis et al. because this would provide a matrix display system which offers improved display quality when displaying moving image (column 2, lines 22-24).

Allowable Subject Matter

8. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Dependent claim 7 identifies a uniquely distinct feature "said operation circuit unit further includes a data-synthesis circuit which combines the pattern data stored in said memories and display data supplied from the exterior of said display device to generate synthesized pattern data, said data driver operating in accordance with the synthesized pattern data to control said display unit to display an image corresponding to the synthesized pattern data".

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (571) 272-7692. The examiner can normally be reached on from Monday to Friday between 10:OOAM and 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (571) 272-7691.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(571) 273-8300 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park 11, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Art unit 2674

Date 11/28/2006

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600